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Application Serial No. 10/577,017
Reply to office action of July 11, 2008

PATENT
Docket: CU-4798

Amendments To The Specification

Please replace the paragraph in the specification on page 27, line 28 to page 28, line 4 with the following amended paragraph:

As shown in FIG. 4C, openings 37 are formed in predetermined positions in the first insulation layer [[25]] --26-- corresponding to the rewiring layers 23. While each opening 37 is formed on an end of the corresponding rewiring layer 23 opposite to the end connected to the post electrode 22A, the opening 37 may be formed in an arbitrary position. It is to be noted that the openings 37 can be formed by etching, laser processing, or the like.

Please replace the paragraph in the specification on page 28, line 21 to page 29, line 5 with the following amended paragraph:

In the post electrode forming process performed after the integrating process, the substrate post electrodes 22A are formed inside the through holes 31A. Since these post electrodes 22A are formed directly on the barrier metal portions 14 (electrodes 13) of the semiconductor chip 11, impedance between the semiconductor chip 11 and the interposer 20A can be reduced, thereby improving electrical properties. Moreover, since the post electrodes 22A are formed using the through holes 31A (on whose inner surface the first insulation layer 25 is actually formed) formed in the interposer base 21A as molds, the post electrodes 22A can be easily formed.

Please replace the paragraph in the specification on page 33, lines 5-14 with the following amended paragraph:

Barrier metal portions 14 are exposed at the bottom of the through holes. Then, copper plating is performed to form the post electrodes [[22A]] --22B-- inside the through holes formed in the dry film. The post electrodes [[22A]] --22B-- are formed directly on the barrier metal portions 14 (electrodes 13). The dry film is then removed, so that the semiconductor chip 11 on which the post electrodes 22B are formed as shown in FIG. 8A is manufactured.

Please replace the paragraph in the specification on page 33, lines 15-29 with

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the following amended paragraph:

After the post electrode forming process is completed, the integrating process is performed. In the integrating process, the semiconductor chip 11 and the interposer base [[21B]] --21A-- are placed in a vacuum unit, and smooth surfaces (mirror surfaces) of the semiconductor chip 11 and the interposer base 21A are brought into contact with and pressed against each other in a predetermined vacuum environment. The smooth surfaces are thus put in tight contact with each other and integrated with each other without using adhesive or the like. As a result, as shown in FIG. 8B, the semiconductor chip 11 and the interposer base [[21B]] --21A-- are securely joined together.

Please replace the paragraph in the specification on page 33, line 30 to page 34, line 6 with the following amended paragraph:

When the semiconductor chip 11 and the interposer base [[21B]] --21A-- are integrated with each other, the post electrodes 22B are inserted in the through holes 31A formed in the interposer base 21A. The diameter of the post electrodes 22B is smaller than the diameter of the through holes 31A, and therefore gaps are formed between the outer circumferential surfaces of the post electrodes 22B and the inner circumferential surfaces of the through holes 31A.

Please replace the paragraph in the specification on page 36, lines 25-31 with the following amended paragraph:

As in the case of the semiconductor device 10D of the [[third]] --fourth-- embodiment, the semiconductor device 10E of this embodiment is configured such that plural post electrodes 22B are disposed in one through hole 31B. The post electrodes 22B are formed directly on barrier metal portions 14 (electrodes 13).

Please replace the paragraph in the specification on page 39, lines 2-12 with the following amended paragraph:

The following describes fifth, sixth, seventh, eighth, ninth, and tenth embodiments of the DURACONTM
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